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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,902	11/27/2002	Tse-Hsiang Hsu	MTKP0029USA	5303

27765 7590 03/22/2006

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EXAMINER	
WONG, LINDA	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,902	HSU, TSE-HSIANG	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-20* is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 1** is objected to because of the following informalities:

   a. **Claim 1**, line 16, recites the limitation "the circuit and ground". There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1, 3-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Knoll et al (US Patent No.: 6546059) in view of Chen et al (US Patent No.: 6744292).

   a. **Claim 1**, Knoll et al discloses a first input current source (Fig. 4, label +Vs) electrically connected to a first node of the circuit (Fig. 4, node above label Iup) supplying a first current (Fig. 6, output from label charge pump1) to the circuit, a second input current source (Fig. 4, label +Vs) electrically connected to a second node of the circuit (Fig. 4, node above label Iup) for supplying a second current to the circuit (Fig. 6, output from label charge pump 2), a first output current source (Fig. 6, label delta Ich and charge pump1) electrically connected

to a third node of the circuit (Fig. 6, node above label delta Ich and charge pump1) for outputting the first current from the circuit (Fig. 6, output from label delta Ich and charge pump 1), a second output current source (Fig. 6, label delta Ich and charge pump 2) electrically connected to a fourth node of the circuit (Fig. 6, node above label delta Ich and charge pump 2) for outputting the second current from the circuit (Fig. 6, output from label delta Ich and charge pump 2), a first capacitor (Fig. 6, label 606) electrically connected between the intermediate node of the circuit (Fig. 6, label 606) and +Vs (Fig. 6, label 606), a unit gain buffer (Fig. 6, label 602) electrically connected between an intermediate node (Fig. 6, node before label 602) and a fifth node of the circuit for (Fig. 6, node after label 602) supplying a voltage of the intermediate node to the fifth node, a resistor (Fig. 6, label R) connected between the buffer (Fig. 6, label 602) and the second charge pump (Fig. 6, label charge pump 2). Although Knoll et al does not show a plurality of switches, Chen et al discloses a plurality of up pulse switches controlled by an up pulse control signal (Fig. 6, labels 68 and 72) for controlling current flow such that in a charging mode of the circuit, wherein the switches are controlled by the output from the phase detector (Col. 1, lines 21-43) and depending on the controls from the phase detector the second current (Fig. 6, output from label 60) flows from the second node through the output node and through the resistor (Fig. 6, label 76) to the fifth node, and the first current (Fig. 6, output from label 64) flows from the first node through the intermediate node to the first capacitor (Fig. 6, label 78) for

charging the first capacitor, and a plurality of down pulse switches (Fig. 6, labels 70 and 74) controlled by a down pulse control signal for controlling current flow such that in a discharging mode of the circuit, where in the switches are controlled by the phase detector and depending on the output from the phase detector (Col. 1, lines 21-43) the second current (Fig. 6, output from label 60) flows from the fifth node through the resistor (Fig. 6, label 76) and out through the second output current source (Fig. 6, label 62), and the first current (Fig. 6, output from label 64) flows from the first capacitor (Fig. 6, label 78) through the intermediate node and out through the first output current source (Fig. 6, label 66) for discharging the first capacitor. Although Knoll et al does not explicitly state a first and second current are equivalent to a predetermined current and a factor, Chen et al also discloses the first current being equal to a predetermined amount of current multiplied by a first factor (Fig. 6, label N-1/N*I), and the second current being equal to the predetermined amount of current multiplied by a second factor (Fig. 6, label I, factor=1). Although Knoll et al discloses a capacitor connected between the first current source and +Vs (Fig. 6, label 606), Chen et al discloses a capacitor connected between the first current source and ground. (Fig. 6, label 78) It would be obvious to one skilled in the art to incorporate Chen et al's invention into Knoll et al's invention to provide smaller current through the capacitor allowing the capacitor to be much smaller in size to match design requirements. (Abstract and Col. 1, lines 44-50)

b. **Claim 3**, Chen et al discloses the plurality of up pulse switches comprises a first up pulse switch and a second up pulse switch (Fig. 6, labels 68 and 72), the first up pulse switch being connected between the first node and the intermediate node (Fig. 6, label 72), and the second up pulse switch being connected between the second node and the output node (Fig. 6, label 68), and the plurality of down pulse switches (Fig. 6, labels 70 and 74) comprises a first down pulse switch and a second down pulse switch (Fig. 6, labels 70 and 74), the first down pulse switch being connected between the intermediate node and the third node (Fig. 6, label 74), and the second down pulse switch being connected between the output node and the fourth node (Fig. 6, label 70).

c. **Claim 4**, Chen et al discloses when the up pulse control signal is active (Col. 1, lines 21-42) and the capacitor starts to charge which would inherently put the circuit in charging mode, the first and second up pulse switches close (Fig, 6, labels 68 and 72) and the first and second down pulse switches open (Fig. 6, labels 70 and 74) and when the down pulse control signal is active (Col. 1, lines 21-42) and the capacitor would inherently start to discharge and the circuit will be in discharging mode, the first and second down pulse switches close and the first and second up pulse switches open (Fig. 6, labels 68,70,72,74).

d. **Claim 5**, Chen et al discloses the first factor is less than one, depending on N (Fig. 6, label N-1/N) and the second factor is equal to one (Fig. 6, label I).

e. **Claim 6**, Chen et al discloses an equivalent circuit to Fig. 6 in Fig. 5, wherein the up pulse switches and the down pulse switches are transistors. (Fig. 5)

f. **Claim 7**, Although Knoll et al fails to discloses a unit gain buffer is a source follower or an emitter follower, Il et al discloses a variable gain amplifier adjusted by a gain control (Fig. 6, label 602) and it would be obvious to one skilled in the art to replace the amplifier as disclosed by Knoll et al based on the designer's choice.

g. **Claim 8**, Although Knoll et al fails to teach a unit gain buffer is an operational amplifier with direct feedback, forming a voltage follower, Knoll et al discloses a variable gain amplifier adjusted by a gain control (Fig. 6, label 602) and it would be obvious to one skilled in the art to replace the amplifier as disclosed by Knoll et al with a feedback operational amplifier based on designer's choice.

3. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Knoll et al (US Patent No.: 6546059) in view of Chen et al (US Patent No.: 6744292).

a. **Claim 2**, although Knoll et al and Chen et al fails to discloses a second capacitor, Gillig et al discloses a resistor (Fig. 2, labels R2 and R1) connected between the first and second charge pump (Fig. 2, labels low current pump charge and high current pump charge) and a capacitor (Fig. 2, label C0) connected to the resistor, ground and the second charge pump. (Fig. 2, labels R2, R1, high current pump charge and C0) It would be obvious to one skilled in the art to incorporate Gillig et al's invention into Knoll et al and Chen et al's invention to provide efficient locking using good spectral purity. (Col. 1, lines 13-52)

Allowable Subject Matter

4. **Claims 9-20** are allowed over prior art.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. Palmer et al (US Patent No.: 5592120)

   b. Duffy et al (US Patent No.: 6385265)

   c. Shenoy et al (US Patent No.: 6169458)

   d. Goldman (US Patent No.: 6611176)

   e. Babanezhad et al (US Patent No.: 5936445).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong

DACHA
PRIMARY EXAMINER